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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,837	03/05/2002	Bruce LaVigne	100202408-1	8627

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EXAMINER	
DYKE, KERRI M	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,837	LAVIGNE ET AL.	
	Examiner	Art Unit	
	Kerri M. Dyke	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 7, filed 02/27/2006, with respect to the drawings have been fully considered and are persuasive. The objection of the drawings has been withdrawn.

2. Applicant's arguments filed 02/27/2006 have been fully considered but they are not persuasive.

3. Applicant's first argument is Budiardjo does not assign a packet to one of multiple queues based on an attribute, wherein each of the queues has a unique priority assigned to it. Figure 1 shows multiple queues, a, b, and c and it is stated "Pi will place packets with smallest RJ values in buffer a, while packets with larger RJ values will be placed in buffers b or c." Therefore, input processor does evaluate an attribute and places the smallest RJ values in queue a, middle values in queue b, and largest values in queue c.

4. Applicant's second argument is that Budiardjo does not perform input pre-processing in a fixed amount of time. Section 3 states, "EF should have the ability to guarantee the packet forwarding rate with minimum packet queue. We implement this property by separating between the input and output processing of packets in the router." In order to achieve the guaranteed rate the input pre-processing must be done in a fixed amount of time.

5. Applicant's third argument is that Budiardjo does not subsequently perform variable latency processing after the packet is forwarded from the memory. Section 3 states, "Po forward packets *taken from buffers*..." (emphasis added). Therefore, Po performs the variable latency processing after taking the packet from memory.

6. Applicant' fourth argument is that Budiardjo teaches away from the embodiments of the present invention because an attribute of the packet is not determined in the first processor. Budiardjo states in section 2, "each incoming packet is time stamped by Pi and then the remaining jitter (RJ) is calculated." RJ is then used to determine the proper queue placement. Therefore, a first processor coupled to the input port determines an attribute. (The input processor, Pi, was mistakenly referred to as the input port in page 4 of the office action. The mistake has been corrected.)

7. In response to applicant's arguments against the references individually (page 18), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

8. Narayana teaches a method of allocating packets among buffers. Teaching a way is not the same as teaching away. Narayana does not provide any teaching to lead one of ordinary skill away from the combination of Budiardjo and Narayana.

9. In response to applicant's argument that Narayana allows packets from various input ports to be simultaneously directed through a switch in a non-blocking manner, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

10. For similar reasons as Narayana, Gorshe does not teach away simply because his embodiments seem to be limited to optical networks. The instant application does not exclude optical networks and there is no teaching to lead one of ordinary skill away from using the

teachings of Gorshe in a network that is not optical. Also similarly to above, a different motivation cannot be the basis for patentability.

11. The contents of the previous office action are reprinted below with updates in order to incorporate the current amendments.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-2, 4, 7-8, 10-13, 15-17, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Budiardjo et al.

14. In regards to claim 1, Budiardjo discloses a system for performing an input processing function on a data packet comprising: an input port; a first processor coupled to said input port wherein said first processor performs said input processing function on said data packet to determine an attribute of said data packet; and a memory coupled to an output of said first processor and having a plurality of queues, each said queue having a unique priority association, wherein said data packet is assigned to one of said plurality of queues and stored in said memory based upon said attribute, wherein said input processing is performed in a fixed amount of time and variable latency processing operations are performed after said data packet is forwarded from said memory based on said priority association to a second processor. Figure 1 discloses an input processor coupled to a memory that contains a plurality of queues with different priorities. It is inherent that there is an input port coupled to the input processor, otherwise data would not

be able to enter the system. Section 3 discloses that the input processor determines the priority of the packet based upon the RJ value. (An explanation of the RJ value is in section 2.) Section 3 also discloses that the router configuration shown in figure 1 is able to guarantee a packet-forwarding rate. Since the forwarding rate is set and guaranteed, the processing must be performed within a fixed amount of time, the amount of time chosen to conform to the guaranteed forwarding rate. Further support for the fact that processing must take a fixed amount of time is found in section 4, where it is disclosed that "assigning the input and output function into two separate processors (Pi and Po) yield to stable packet forwarding rate, independent of the arrival pattern of incoming packets." As stated in section 3 the number of packets taken from the buffers is related to the RJ value, which is used to determine priority.

15. In regards to claim 2, Budiardjo discloses the system as recited in claim 1 wherein said attribute comprises an indicator of a priority characterizing said data packet (section 3).

16. In regards to claim 4, Budiardjo discloses the system as recited in claim 1, wherein said system functions in concert with said second processor (output processor, figure 1).

17. In regards to claim 7, Budiardjo discloses the system as recited in claim 1 wherein said memory functions as an input buffer (Figure 1 shows the memory as being buffers a, b, and c).

18. In regards to claim 8, Budiardjo discloses a method for performing an input process on a data packet comprising: pre-processing said data packet to determine a characteristic of said data packet before said data packet is subjected to input buffering, wherein said pre-processing comprises a fixed time processing operation; determining one of a plurality of queues within a memory in which to store said data packet according to said characteristic, wherein each said queue has a unique priority association and wherein said pre-processing is performed in a first

processor coupled to an input of said memory; and storing said data packet in said queue; based on said determining wherein said storing comprises an input buffering function that is performed prior to forwarding said data packet, based on said priority association, for subsequent processing in a second processor. Section 3 discloses determining a characteristic of the data packet and using said characteristic to choose the appropriate buffer. After the characteristic and appropriate queue is determined the data packet is placed in the appropriate queue. Figure 1 discloses an input processor coupled to a memory that contains a plurality of queues with different priorities. It is inherent that there is an input port coupled to the input processor, otherwise data would not be able to enter the system. Section 3 discloses that the input processor determines the priority of the packet based upon the RJ value. (An explanation of the RJ value is in section 2.) Section 3 also discloses that the router configuration shown in figure 1 is able to guarantee a packet-forwarding rate. Since the forwarding rate is set and guaranteed, the processing must be performed within a fixed amount of time, the amount of time chosen to conform to the guaranteed forwarding rate. Further support for the fact that processing must take a fixed amount of time is found in section 4, where it is disclosed that "assigning the input and output function into two separate processors (Pi and Po) yield to stable packet forwarding rate, independent of the arrival pattern of incoming packets." As stated in section 3 the number of packets taken from the buffers is related to the RJ value, which is used to determine priority.

19. In regards to claim 10, Budiardjo discloses the method as recited in claim 8 wherein said first processor comprises an input pre-processor. Figure 1 shows the input processor, Pi. Pi is labeled as an input processor, but the processing is done before the packet is placed in a queue, making it an input preprocessor.

20. In regards to claim 11, Budiardjo discloses the method as recited in claim 10 wherein said first processor passes said data packet through to said queue further comprises pipelining said data packet substantially free of variable latency. Section 3 discloses that the packet is forwarded with a guaranteed rate. In order to meet this rate the packet must be queued without variable delay. If the queuing delay was variable then the system would not be able to predict and guarantee a rate of service.

21. In regards to claim 12, Budiardjo discloses the method as recited in claim 11 wherein said forwarding comprises an operation wherein said data packet is transferred from said queue within said memory to said second processor (section 3).

22. In regards to claim 13, Budiardjo discloses the method as recited in claim 8 wherein said forwarding enables said memory to utilize a full bandwidth of an input port coupled to said first processor. In sections 4 and 5 Budiardjo discloses that packet loss from the system is well below 8%. This means that the packet forwarding system is working effectively to prevent the backup of the input port and therefore the full bandwidth of the input port is utilized.

23. In regards to claim 15, Budiardjo discloses a system for performing input processing on a data packet comprising: means for determining an attribute of said data packet (section 2); and means for storing said data packet wherein said storing means comprises a plurality of queues, wherein each of said queues has a unique associated priority, wherein said data packet is stored in one of said queues according to said attribute, and wherein said input processing is performed in a fixed amount of time, wherein variable latency processing operations are performed after said data packet is forwarded from said memory, based on said associated priority, to subsequent processing means. Figure 1 discloses an input processor coupled to a memory that contains a

plurality of queues with different priorities. It is inherent that there is an input port coupled to the input processor, otherwise data would not be able to enter the system. Section 3 discloses that the input processor determines the priority of the packet based upon the RJ value. (An explanation of the RJ value is in section 2.) Section 3 also discloses that the router configuration shown in figure 1 is able to guarantee a packet-forwarding rate. Since the forwarding rate is set and guaranteed, the processing must be performed within a fixed amount of time, the amount of time chosen to conform to the guaranteed forwarding rate. Further support for the fact that processing must take a fixed amount of time is found in section 4, where it is disclosed that "assigning the input and output function into two separate processors (Pi and Po) yield to stable packet forwarding rate, independent of the arrival pattern of incoming packets." As stated in section 3 the number of packets taken from the buffers is related to the RJ value, which is used to determine priority.

24. In regards to claim 16, Budiardjo discloses the system as recited in claim 15 wherein said determining means comprises: means for processing said data packet; and means for pipelining said data packet into said queue (Pi, figure 1).

25. In regards to claim 17, Budiardjo discloses the system as recited in claim 15 wherein said system functions substantially free of variable latency. Section 4 discloses that the system yields stable packet forwarding rates. Stable rates indicate that the rates are not variable, therefore there cannot be variable latency within the system.

26. In regards to claim 19, Budiardjo discloses the system as recited in claim 15 wherein said storing means comprises means for buffering said data packet (figure 1).

Claim Rejections - 35 USC § 103

27. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 3, 9, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Budiardjo et al. in view of applicant admitted prior art.

29. In regards to claim 3, Budiardjo discloses the system as recited in claim 1, but not wherein said attribute comprises at least one of: a type characterizing said data packet; encapsulation of said data packet; a priority corresponding to a tag comprising said data packet; a priority corresponding to another criterion; an Internet Protocol header identity; a Transfer Control Protocol header identity; a class assigned to said data packet; a class of service rating assigned to said data packet; a quality of service assigned to said data packet; and a differentiated services field.

Applicant admits it is well known to use a class of service rating assigned to a data packet in page 2 lines 9-16.

It would have been obvious to one of ordinary skill in the art to use COS to assign packets to a queue because COS indicates QoS parameters which must be satisfied by the network, as taught by Budiardjo in section 2.

30. Claim 9 is rejected upon the same grounds as claim 3.

31. Claim 18 is rejected upon the same grounds as claim 3.

32. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Budiardjo et al. in view of Narayana et al. (US 6,469,983).

33. In regards to claims 5 and 6, Budiardjo discloses the system of claim 1. Budiardjo does not disclose using a network control protocol or that protocol being a media access control layer.

Narayana discloses using a MAC layer, which is a type of network control protocol in figure 3.

It would have been obvious to one of ordinary skill in the art to use a network control protocol such as a MAC, because doing so is well known in the art and is actually required by most packet protocols.

34. Claims 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Budiardjo et al. in view of Gorshe (US 5,412,651).

35. In regards to claim 14, Budiardjo discloses the method as recited in claim 8, but not wherein said memory effectively buffers subsequent processing of said data packet.

Gorshe discloses buffering subsequent processing of the data packet in column 3 lines 53-54.

It would have been obvious to one of ordinary skill in the art to buffer the subsequent processing of the data packet because doing so increases the efficiency of the system, as disclosed by Gorshe in column 3 line 66 – column 4 line 18.

36. In regards to claim 20, Budiardjo discloses the system as recited in claim 19 but not wherein said buffering means functions to buffer a subsequent processing operation wherein said subsequent processing operation comprises at least one of a fixed and a variable latency.

Gorshe discloses buffering subsequent processing of the data packet in column 3 lines 53-54. Although Gorshe does not disclose the subsequent processing is selectively fixed or variable latency it is inherent that the subsequent processing must be one of the two because they are the only two options. Processing can either take a fixed or variable amount of time.

It would have been obvious to one of ordinary skill in the art to buffer the subsequent processing of the data packet because doing so increases the efficiency of the system, as disclosed by Gorshe in column 3 line 66 – column 4 line 18.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kerri M. Dyke whose telephone number is (571) 272-0542. The examiner can normally be reached on Monday through Friday, 7:00 am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (571) 272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

kmd

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